* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The value (semi- cusp value) in which the envelope of a signal (Sin) carried out weighting The semi- cusp value detector for detecting Are (1) and the process about :charged-capacitor (C) The digital discharge filter which carries out simulation of the process about the digital charge filter (4); discharge capacitor (C) which carries out simulation (8); Connected with the lower stream of a river of said digital charge filter (4) and said digital discharge filter (8). A semi- cusp value detector equipped with digital attenuation filter (6); which carries out simulation of the attenuation response of a metering device.
[Claim 2] A digital charge filter (4) and a digital discharge filter (8) are a semi- cusp value detector according to claim 1 which takes the form of the primary IIR (infinity impulse response) filter, and is characterized by each materializing the primary low pass filter.
[Claim 3] Said primary IIR (infinity impulse response) filter The delay element which it has between two adders (25 27) and said adder (25 27) (28), The feedback multiplier multiplier (29) which connects to the adder (25) of an input side two input loading factor multipliers (24 26) which connect the input (IN) of said IIR filter one of said the adders (25 27) in each case, and the adder (27) of an output side is included. It is the semi- cusp value detector according to claim 2 characterized by the multiplier (b1, b2) of the input loading factor multiplier (24 26) about a digital discharge filter (8) serving as zero in it.
[Claim 4] Said digital attenuation filter (6) is a semi- cusp value detector according to claim 1 to 3 characterized by taking the form of the secondary IIR (infinity impulse response) filter, and materializing the primary two united low pass filters attenuated in criticality.
[Claim 5] Said secondary IIR (infinity impulse response) filter Two delay elements which it has between three adders (16, 17, 18) and said adder (16, 17, 18) (19 20), Three input loading factor multipliers which connect the input (IN) of said IIR filter one of said the adders (16, 17, 18) in each case (21, 22, 23), And two feedback multiplier multipliers (14 15) which connect the adder (18) of an output side to one of the adders (16 17) of other except it in each case are included. And the multiplier (b1, b3) of the input loading factor multiplier (23) which connects to the adder (18) of an output side the input loading factor multiplier (21) which connects said input (IN) to the adder (16) of an input side in it, and said input (IN) is a semi- cusp value detector according to claim 4 characterized by the equal thing.
[Claim 6] The semi- cusp value detector according to claim 1 to 5 characterized by equipping the upstream of said digital charge filter (4) and said digital discharge filter (8) with a digital input filter (2a).
[Claim 7] Said digital input filter (2a) is a semi- cusp value detector according to claim 6 characterized by taking the form of the secondary IIR (infinity impulse response) filter.
[Claim 8] The semi- cusp value detector according to claim 6 or 7 characterized by having an absolute value generator (2b) between said digital input filter (2a) and said digital charge filter.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the so-called semi- cusp value detector. A semi- cusp value detector is useful when detecting the peak value in which the envelope of a signal, for example, the envelope of the signal of an intermediate frequency stage, carried out weighting.
[0002]
[Description of the Prior Art] A semi- cusp value detector changes the envelope of an electric noise electrical potential difference into the output-signal level which suited the physical consciousness response of human being's lug or human being's eye. This kind of semi- cusp value detector is explained by "IEC CISPR 16-1 / 1999-10", "Specification of Radio Disturbance and Immunity Measuring Apparatus and Method" (radio interference, immunity metering-device, and specification of approach), and part I: "Radio Disturbance and Immunity Measuring Apparatus" (radio interference and immunity metering device) in full detail. Human being's lug or human being's eye senses the interference pulse concerned much more troublesome, so that the interference pulse of the same amplitude is repeated at a high rate. The purpose of a semi- cusp value detector is to carry out simulation of this subjective consciousness response of human being's lug or human being's eye.
[0003] Drawing 2 shows behavior of the semi- cusp value detector demanded in the above-mentioned specification. Here, the noise electrical potential difference of the input side which in each case is needed in order to obtain an equal output level in the output of a semi- cusp value detector is expressed as a function of the pulse rate (rate of a repeat) of a noise electrical potential difference. In this drawing, in order to obtain a specific output level, it can recognize that a semi- cusp value detector needs a high noise electrical potential difference in a lower pulse rate compared with the case of a higher pulse rate. If another expression is used, it can be said that a semi- cusp value detector becomes high sensitivity more to a noise electrical potential difference with a comparatively high pulse rate.
[0004] The semi- cusp value detector is constituted for some time by the analog-design by the approach of becoming clear from drawing 1 . About this, it will be Hewlett in May, 1986, for example. It can know from "Application Note HP-AN 331-1" (application note HP-AN 331-1) published by Packard (Hewlett Packard). It is rectified in Diode D and Sin is supplied to Capacitor C through the charge resistance R1. Between each half wave of an input signal Sin, Capacitor C is charged through the charge resistance R1 according to it. Discharge of Capacitor C is hung down through the discharge resistance R2 connected to Capacitor C and juxtaposition. It is possible to carry out direct continuation of a metering device, for example, the moving iron type measuring instrument, on the lower stream of a river of Buffer B, and the instrumentation of at the time in early stages of semi- cusp value measurement was carried out mainly according to this approach. More newly, evaluation came to be performed electronically generally and analog low pass filter T3 which carries out simulation of the response of a metering device was connected to the lower stream of a river of Buffer B. As that result, the time constant which this circuit has is the damping time constant tau 3 of : used as the following three, i.e., charge time constant tau1=R1 and C, discharge time constant tau2=R2 and C, and damping element T3.
[0005]
[Problem(s) to be Solved by the Invention] In order to be, :, i.e., the exact measurement, which the following problems have produced with regards to implementation by the analog of a semi- cusp value detector, it is that compensation of Diode D becomes indispensable. If a capacitor must be quality and it puts in another way for reasons of the big discharge time constant tau 2, a charge must be able to be held over a comparatively long period (several seconds), without being accompanied by big loss. As shown in drawing 2 , a circuit which the appointed sensibility differs when frequency bands differ, therefore is different for every frequency band needs to be used for a semi- cusp value detector. Achievement is difficult for long term stability and temperature

stability. It turned out that tuning and range change of a detector are difficult after all.
[0006] Therefore, the purpose which makes the foundation of this invention is making a semi- cusp value detector without the above-mentioned fault, and especially the semi- cusp value detector concerned shall have high long term stability and temperature stability, and shall be usable in each frequency band, and shall not need adjustment.
[0007]
[Means for Solving the Problem] This purpose is attained by the description of a claim according to claim 1.
[0008] According to this invention, the application replaced with the analog component which showed the attenuation response of the digital charge filter which carries out simulation of the process about charge of a capacitor, the digital discharge filter which carries out simulation of the process about discharge of a capacitor, and a metering device to the digital attenuation filter which carries out simulation at drawing 1 is found out. Implementation of the semi- cusp value detector by digital one enables measurement accompanied by a high precision.
[0009] The dependent claim includes the further development advantageous in the semi- cusp value detector by this invention.
[0010] The multiplier of being able to mount a digital charge filter and a digital discharge filter as primary IIR (infinity impulse response) filter, setting them in that case, and the input voltage about a discharge filter becoming equal to zero, consequently setting the multiplier of an input side to zero or an input side is omissible.
[0011] A digital attenuation filter can take the form of the secondary IIR (infinity impulse response) filter, and can materialize the primary two united low pass filters attenuated in criticality. In this case, two multipliers become the same.
[0012] A digital input filter can be similarly materialized as secondary IIR (infinity impulse response) filter.
[0013] The semi- cusp value detector of this invention Thus, a passage according to claim 1, The value (semi- cusp value) in which the envelope of a signal (Sin) carried out weighting The semi- cusp value detector for detecting Are (1) and the process about :charged-capacitor (C) The digital discharge filter which carries out simulation of the process about the digital charge filter (4); discharge capacitor (C) which carries out simulation (8); Connected with the lower stream of a river of said digital charge filter (4) and said digital discharge filter (8). It has digital attenuation filter (6); which carries out simulation of the attenuation response of a metering device. Moreover, a semi- cusp value detector according to claim 2 takes the form of the primary IIR (infinity impulse response) filter in a semi- cusp value detector according to claim 1, and, as for a digital charge filter (4) and a digital discharge filter (8), each is characterized by materializing the primary low pass filter. A semi- cusp value detector according to claim 3 is set to a semi- cusp value detector according to claim 2. Moreover, said primary IIR (infinity impulse response) filter The delay element which it has between two adders (25 27) and said adder (25 27) (28), The feedback multiplier multiplier (29) which connects to the adder (25) of an input side two input loading factor multipliers (24 26) which connect the input (IN) of said IIR filter one of said the adders (25 27) in each case, and the adder (27) of an output side is included. It is characterized by the multiplier (b1, b2) of the input loading factor multiplier (24 26) about a digital discharge filter (8) serving as zero in it. Moreover, a semi- cusp value detector according to claim 4 is characterized by for said digital attenuation filter (6) taking the form of the secondary IIR (infinity impulse response) filter, and materializing the primary two united low pass filters attenuated in criticality in a semi- cusp value detector according to claim 1 to 3. A semi- cusp value detector according to claim 5 is set to a semi- cusp value detector according to claim 4. Moreover, said secondary IIR (infinity impulse response) filter Two delay elements which it has between three adders (16, 17, 18) and said adder (16, 17, 18) (19 20), Three input loading factor multipliers which connect the input (IN) of said IIR filter one of said the adders (16, 17, 18) in each case (21, 22, 23), And two feedback multiplier multipliers (14 15) which connect the adder (18) of an output side to one of the adders (16 17) of other except it in each case are included. And the multiplier (b1, b3) of the input loading factor multiplier (23) which connects to the adder (18) of an output side the input loading factor multiplier (21) which connects said input (IN) to the adder (16) of an input side in it, and said input (IN) is characterized by the equal thing. Moreover, a semi- cusp value detector according to claim 6 is characterized by equipping the upstream of said digital charge filter (4) and said digital discharge filter (8) with a digital input filter (2a) in a semi- cusp value detector according to claim 1 to 5. Moreover, a semi- cusp value detector according to claim 7 is characterized by said digital input filter (2a) taking the form of the secondary IIR (infinity impulse response) filter in a semi- cusp value detector according to claim 6. Moreover, a semi- cusp value detector according to claim 8 is characterized by having an absolute value generator (2b) between said digital input filter (2a) and said digital charge filter in a semi- cusp value detector according to claim 6 or 7.
[0014]

[Embodiment of the Invention] Hereafter, with reference to a drawing, this invention is explained more to a detail. The gestalt of the operation of the semi- cusp value detector 1 made into an example by this invention at drawing 3 is shown. An input signal Sin is supplied to digital input filter 2a (drawing 5) which has a transfer function Hk (z). Since there is absolute value generator 2b (drawing 5) which derives the absolute value of an output signal in the output of digital input filter 2a, the overall transfer function of the filter block 2 with which digital input filter 2a and absolute value generator 2b were combined serves as abs [Hk (z)].

[0015] The input filter 2 is connected to the digital charge filter 4 through the 1st filter change element 3. The digital charge filter 4 has a transfer function H1 (z), and carries out simulation of the process about charge of the capacitor C accompanied by time constant tau1=R1 and C. The charge cycle of the semi- cusp value detector 1 by this invention is expressed by drawing 3 R> 3. The output of the digital charge filter 4 is connected to the digital attenuation filter 6 through the 2nd filter change element 5. This digital attenuation filter 6 has a transfer function H3 (z), and carries out simulation of the attenuation response of the metering device accompanied by a time constant tau 3. An output signal Sout is acquired in the output of the attenuation filter 6. The final value of the output in the last of a charge process is passed to the digital discharge filter 8 through the 3rd change element 7, and this final value is used as a starting value about a discharge cycle in it. The output of the digital discharge filter 8 changes between the charge cycles shown in drawing 3 , and it is separated from the attenuation filter 6 by the element 5. Furthermore, the 4th change element 9, i.e., the change element which can connect the output of the discharge filter 8 to the input of the charge filter 4 through it, is equipped. However, this change element 9 is opened between the charge cycles shown in drawing 3 .

[0016] Furthermore, it has the control unit 10 and the output voltage X1 of a filter 2 is compared with the input voltage X2 of the attenuation filter 6 in it. When an electrical potential difference X1 is larger than an electrical potential difference X2, a circuit is in a charge cycle and the control unit 10 has changed to the change condition which shows the change elements 3, 5, 7, and 9 in drawing 3 . When an electrical potential difference X2 is larger than an electrical potential difference X1, a circuit is in a discharge cycle and the change elements 3, 5, 7, and 9 are changed to the change position shown in drawing 4 .

[0017] In the change position shown in drawing 4 , the output of a filter 2 is separated from the charge filter 4. Furthermore, either the attenuation filter 6 and the discharge filter 8 are separated for the output of the charge filter 4, and the input of the discharge filter 8 becomes zero potential. It connects with the input of the attenuation filter 6 through the change element 5, and the output of the discharge filter 8 is connected to the input 11 of the charge filter 4 through the change element 9. That is, the final value of the output of the discharge filter 8 in the last of a discharge cycle is passed to the input of the charge filter 4 through the change element 9, consequently can start the charge cycle which continues immediately after this discharge cycle by making this into starting potential.

[0018] Some drawing 5 shows the block diagram of the semi- cusp value detector 1 by this invention using the expression which added correction. The input filter block 2 is divided into absolute value generator 2b connected to input filter 2a and its lower stream of a river. Since the charge filter 4 and the discharge filter 8 can be substantially mounted according to the same approach, these two filters are unified by one filter block 11. The final value of the charge filter 4 is internally guaranteed to its thing [adopting the final value of the discharge filter 8 as a starting value for the charge filter 4 conversely] as a starting value for the discharge filter 8 in the filter block 11. Therefore, in the input of the filter block 11, only the single change element 12 is needed. Moreover, in the gestalt of this operation illustrated here, a detector 10 compares the signal level X1 in the output of absolute value generator 2b with the signal level X2 in the input of the attenuation filter 6. When signal level X1 is larger than signal level X2, the filter block 11 is changed so that the filter block 11 may operate as a charge filter 4. When [that] signal level X2 is conversely larger than signal level X1, the filter block 11 is changed so that the filter block 11 may operate as a discharge filter 8. The maximum generator 13 which determines the maximum of an output signal Sout is connected to the lower stream of a river of the attenuation filter 6.

[0019] Some examples about mounting of digital filters 2a, 4, 8, and 6 are shown in drawing 6 thru/or drawing 8 .

[0020] Drawing 6 is the gestalt of operation shown as an example of input filter 2a. In materializing the semi- cusp value detector 1 in digital one Only the charge RC element which consists of R1 and C in one side, and the discharge RC element which consists of R2 and C in another side are materialized as a digital low pass filter. And it is clear that the behavior shown in drawing 2 is not obtained correctly by having made it shape taken as secondary low pass filter which attenuation filter T3 attenuates in criticality. The input filter 2 corrects the frequency response of a measuring device, in order to gain the measurement bandwidth specified as the criterion. In order to carry out simulation of the behavior shown in drawing 2 as a function of a pulse rate, in input filter 2a, pre filtering of an input signal Sin must be performed first. It turned out that this input filter 2a

must be mounted as an FIR (finite impulse response) accompanied by the delay element (tap) of 63. This mounting is suitable for the somatization using the hardware by ASIC. About the gestalt of the desirable operation illustrated to drawing 6 , input filter 2a is mounted as secondary IIR (infinity impulse response) filter. This mounting becomes what was suitable in somatization for example, by the digital signal processor (DSP).

[0021] As shown in drawing 6 , when materializing input filter 2a as secondary IIR filter, in the conventional approach, it has three adders 16, 17, and 18, and they are mutually connected through the delay elements 19 and 20. Input IN is connected to the 1st adder 16 through the 1st input loading factor multiplier 21 which multiplies the input signal concerned by the 1st input loading factor b3. It connects with the 3rd adder 18 through the 3rd input loading factor multiplier 23 which is connected to the 2nd adder 17 through the 2nd input loading factor multiplier 23 which multiplies the input signal concerned by the 2nd input loading factor b2, and multiplies the input signal concerned by the 3rd input loading factor b1. The output of the 3rd adder 18 is the 1st feedback multiplier to the output signal concerned. - It connects with the 1st adder 16 through the 1st feedback multiplier multiplier 14 which multiplies by a3, and is the 2nd feedback multiplier to the output signal concerned. - It connects with the 2nd adder 17 through the 2nd feedback multiplier multiplier 15 which multiplies by a2. The 1st adder 16 adds the output signal of the multiplier multipliers 21 and 14. The 2nd adder 17 adds the output signal of the delay element 19, and the output signal of the multiplier multipliers 22 and 15. The 3rd adder 18 adds the output signal of the delay element 20, and the output signal of the multiplier multiplier 23. It is necessary to choose multipliers b1, b2, and b3, -a2, and -a3 so that the behavior shown in drawing 2 may be obtained.

[0022] Drawing 7 A shows mounting of the filter block 11 as primary IIR filter. Input IN is connected to the 2nd adder 27 through the 2nd input loading factor multiplier 26 which is connected to the 1st adder 25 through the 1st input loading factor multiplier 24 which multiplies the input signal concerned by the 1st input loading factor b2, and multiplies the input signal concerned by the 2nd input loading factor b1 so that generally [in the case of the primary IIR filter]. The adders 25 and 27 of each other are connected through the delay element 28. The output of the 2nd adder 27 is a feedback multiplier to the output signal of the 2nd adder 27. - It connects with the 1st adder 25 through the feedback multiplier multiplier 29 which multiplies by a2. The 1st adder 25 adds the output signal of the multiplier multipliers 24 and 29. The 2nd adder 27 adds the output signal of the delay element 28, and the output signal of the multiplier multiplier 26.

[0023] When the filter block 11 operates as a charge filter 4, it is necessary to choose multipliers b1 and b2 and -a2 so that the filter block 11 may operate as primary low pass filter. A related representative circuit schematic is shown in drawing 7 B. Capacitor C is charged through resistance R1.

[0024] When the filter block 11 operates as a discharge filter 8, it is necessary to choose equally to zero input loading factors b1 and b2. Therefore, when mounting of the charge filter 4 and mounting of the discharge filter 8 are divided, the multiplier multipliers 24 and 26 can be omitted. A related equal circuit is shown in drawing 7 C. Discharge of the capacitor C through resistance R2 becomes the low pass filter and equivalence with which the input of series resistance R2 is connected to the ground of a circuit. That is, an input signal equal to zero is continuously supplied to a digital filter in this case. The output of the 2nd adder 27 is equipped with the down-sampler (sampling rate converter) which lowers a sampling rate by making N into a factor.

[0025] The attenuation filter 6 can be substantially mounted as secondary IIR filter similarly with input filter 2a, as shown in drawing 8 . The corresponding reference designator is given to the element already explained based on drawing 6 with reference to the explanation relevant to drawing 6 in this connection. Since the attenuation filter 6 consists of the primary united low pass filter which two critical targets (critical) are made to decrease, the 1st input loading factor b3 becomes the same as that of the 3rd input loading factor b1. This becomes clear at drawing 8 .

[0026] Behavior of the semi- cusp value detector 1 by this invention is shown in drawing 9 and 10 based on two examples.

[0027] Drawing 9 A expresses the input signal Sin accompanied by the pulse rate (rate of a repeat) of 1Hz. The area used as the pulse bottom is normalized by 1 in this. The signal X2 corresponding to the input signal Sin expressed to drawing 9 A in the output of the filter block 11 and the output signal Sout in the output of the attenuation filter 6 are expressed to drawing 9 B as a function of time amount t. Behavior of the charge of a serrate form by which simulation was carried out with the charge filter 4 and the discharge filter 8, and discharge can be recognized clearly. The attenuation filter 6 which consists of the primary two united low pass filters 1 attenuated in criticality brings about the decreased wavelike signal Sout.

[0028] Drawing 10 A expresses the input signal Sin accompanied by the pulse rate (rate of a repeat) of 5Hz. The area included by the pulse also in this is normalized by 1. Drawing 10 B expresses the signal X2 in the output of the filter block 11, and the output signal Sout in the output of the attenuation filter 6 like the above-mentioned.

In contrast with the signal Sout shown in drawing 9 B, the signal Sout in this case is seldom influenced of wavelike nature, but is approximated to asymptotic threshold value. In each case, the maximum generator 13 secures the maximum of Signal Sout after the measuring time [finishing / decision / beforehand].

[0029] This invention is not limited to the gestalt of the operation illustrated here. Especially, the somatization using other digital filters, for example, FIR filter, is also possible.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram having shown the basic structure of the semi- cusp value detector of the analog design by the conventional technique.
[Drawing 2] It is a graph aiming at explaining the sensibility of a semi- cusp value detector.
[Drawing 3] It is the block diagram having shown the gestalt of operation of the 1st change condition of the semi- cusp value detector by this invention.
[Drawing 4] It is the block diagram having shown the gestalt of operation of the 2nd change condition of the semi- cusp value detector shown in drawing 3 .
[Drawing 5] It is the block diagram having shown the gestalt of operation of the semi- cusp value detector by this invention.
[Drawing 6] It is the block diagram having shown somatization of the input filter in the gestalt of the operation illustrated to drawing 3 thru/or drawing 5 .
[Drawing 7] (drawing 7 A) It is the block diagram having shown somatization of the charge filter in the gestalt of the operation illustrated to drawing 3 thru/or drawing 5 , or a discharge filter. (drawing 7 B) It is the representative circuit schematic of a charge filter. (drawing 7 C) It is the representative circuit schematic of a discharge filter.
[Drawing 8] It is the block diagram having shown somatization of the attenuation filter in the gestalt of the operation illustrated to drawing 3 thru/or drawing 5 .
[Drawing 9] (drawing 9 A) It is the graph which showed the interference signal accompanied by the pulse rate of 1Hz. (drawing 9 B) The input signal when being shown in drawing 9 A in the case of the semi- cusp value detector by this invention is the graph which showed the signal of before an attenuation filter and after that.
[Drawing 10] (drawing 10 A) It is the graph which showed the interference signal accompanied by the pulse rate of 5Hz. (drawing 10 B) The input signal when being shown in drawing 10 A in the case of the semi- cusp value detector by this invention is the graph which showed the signal of before an attenuation filter and after that.
[Description of Notations]
2 Input Filter
2a Digital input filter
2b Absolute value generator 2b
3 1st Filter Change Element
4 Digital Charge Filter
5 2nd Filter Change Element
6 Digital Attenuation Filter
7 3rd Change Element
8 Digital Discharge Filter
9 4th Change Element
10 Control Unit
11 Filter Block
12 Change Element
13 Maximum Generator
14 1st Feedback Multiplier Multiplier
15 2nd Feedback Multiplier Multiplier
16 1st Adder
17 2nd Adder
18 3rd Adder

19 Delay Element
20 Delay Element
21 1st Input Loading Factor Multiplier
23 3rd Input Loading Factor Multiplier
24 1st Input Loading Factor Multiplier
25 1st Adder
26 2nd Input Loading Factor Multiplier
27 2nd Adder
28 Delay Element
Sin Input signal
Sout Output signal
C Capacitor
R1 Charge resistance
R2 Discharge resistance
B Buffer
T3 Analog low pass filter
tau 1 Charge time constant
tau 2 Discharge time constant
tau 3 Damping time constant
Hk (z) Transfer function
X1 Signal level
X2 Signal level

[Translation done.]

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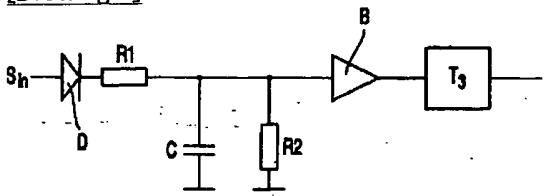
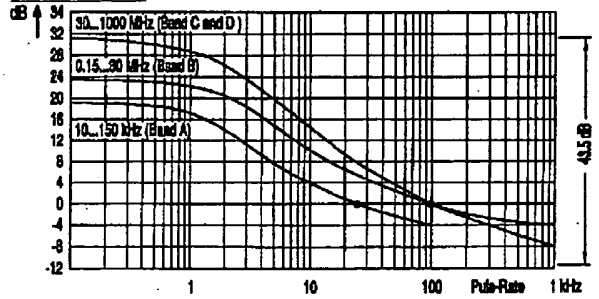
DRAWINGS

[Drawing 1]

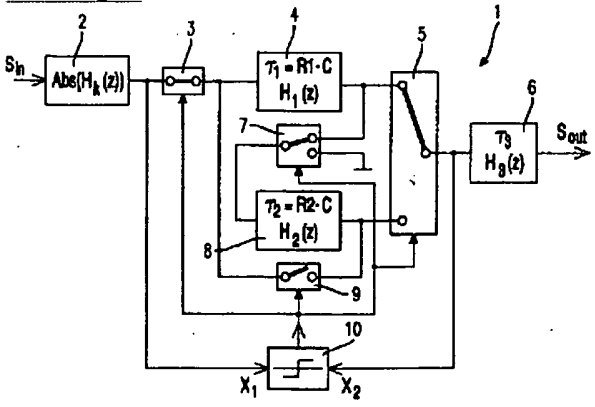


従来技術

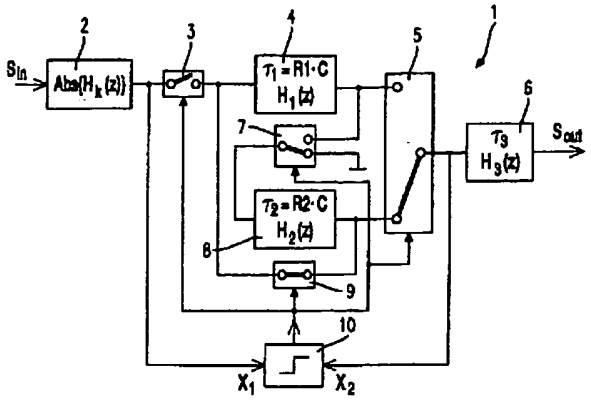
[Drawing 2]



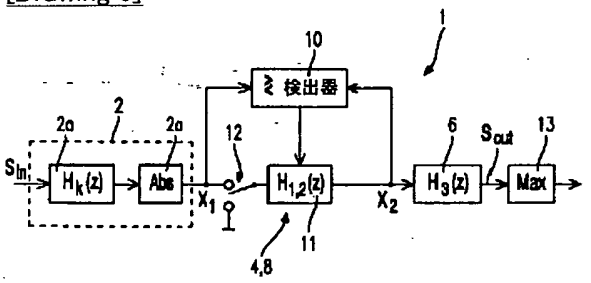
[Drawing 3]



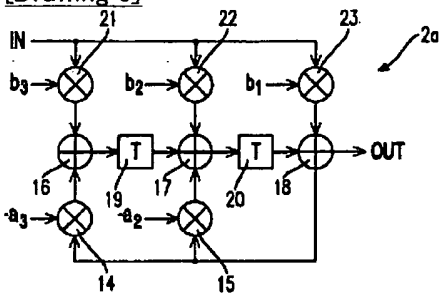
[Drawing 4]



[Drawing 5]

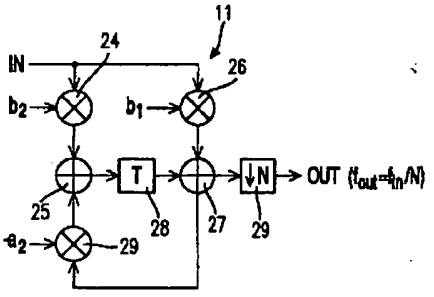


[Drawing 6]

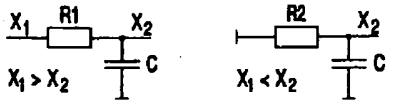


[Drawing 7]

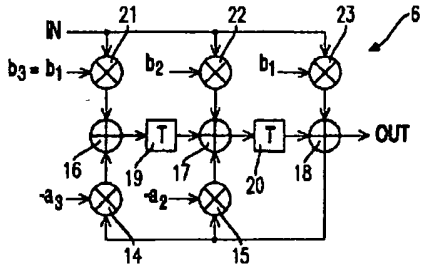
(A)



(B) (C)

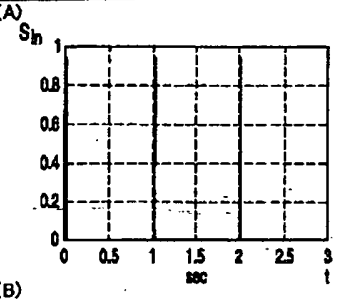


[Drawing 8]

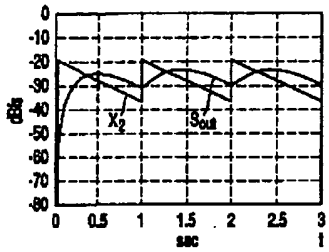


[Drawing 9]

(A)

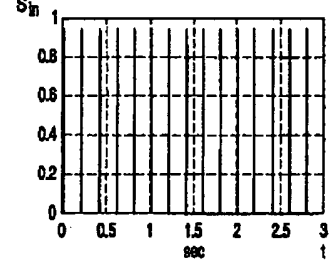


(B)

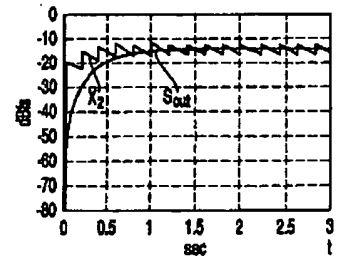


[Drawing 10]

(A)



(B)



[Translation done.]